SONY

CXP85300A/85390A

CMOS 8-bit 1-chip Microcomputer

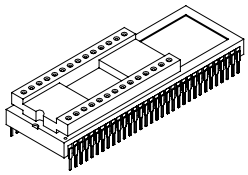
Piggyback/ evaluator type

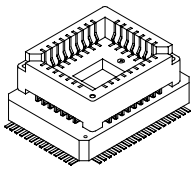
Description

The CXP85300A/85390A are CMOS 8-bit 1-chip microcomputers that serve as both piggyback and evaluator. The CXP85300A/85390A are developed for evaluating the function of the CXP85324A/CXP 85332A/85340A.

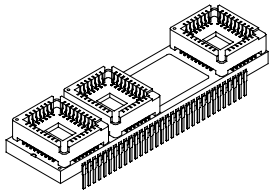
Note that CXP85300A corresponds to the fixed font, and CXP85390A corresponds to the custom font respectively.

64 pin PSDIP (Ceramic) 64 pin PQFP (Ceramic)





64 pin PSDIP (Ceramic)



Features

- Instruction set which supports a wide array of data types
  - — 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle 1µs/4MHz (4MHz version)
  0.5µs/8MHz (8MHz version)
- EPROM 27C512
  LCC type 27C512
- Incorporated RAM capacity 576 bytes
- EPROM for custom font (CXP85390A only)
  LCC type 27C256, LCC type 27C512
  (used volume is 16K bytes)
- Peripheral functions
  - — On-screen display function 12×18 dots, 256 types 15 colors, 21 characters $\times$ 12 lines
    Black frame output half blanking, shadow, background color on full screen/ half blanking
    Double scanning mode, jitter elimination circuit
  - — I^2C bus interface
  - — PWM output 14 bits, 1 channel
    8 bits, 8 channels
  - — Remote control receiving circuit 8-bit pulse measurement counter, 6-stage FIFO
  - — A/D converter 8 bits, 4 channels, successive approximation system
    (conversion time of 40µs/4MHz, 8MHz)
  - — HSYNC counter
  - — Power supply frequency counter
  - — Watchdog timer
  - — Serial I/O 8-bit clock synchronized
  - — Timers 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interrupts 14 factors, 14 vectors multi-interruption possible
- Standby mode Sleep
- Package 64-pin ceramic SDIP/QFP

Structure

Silicon gate CMOS IC

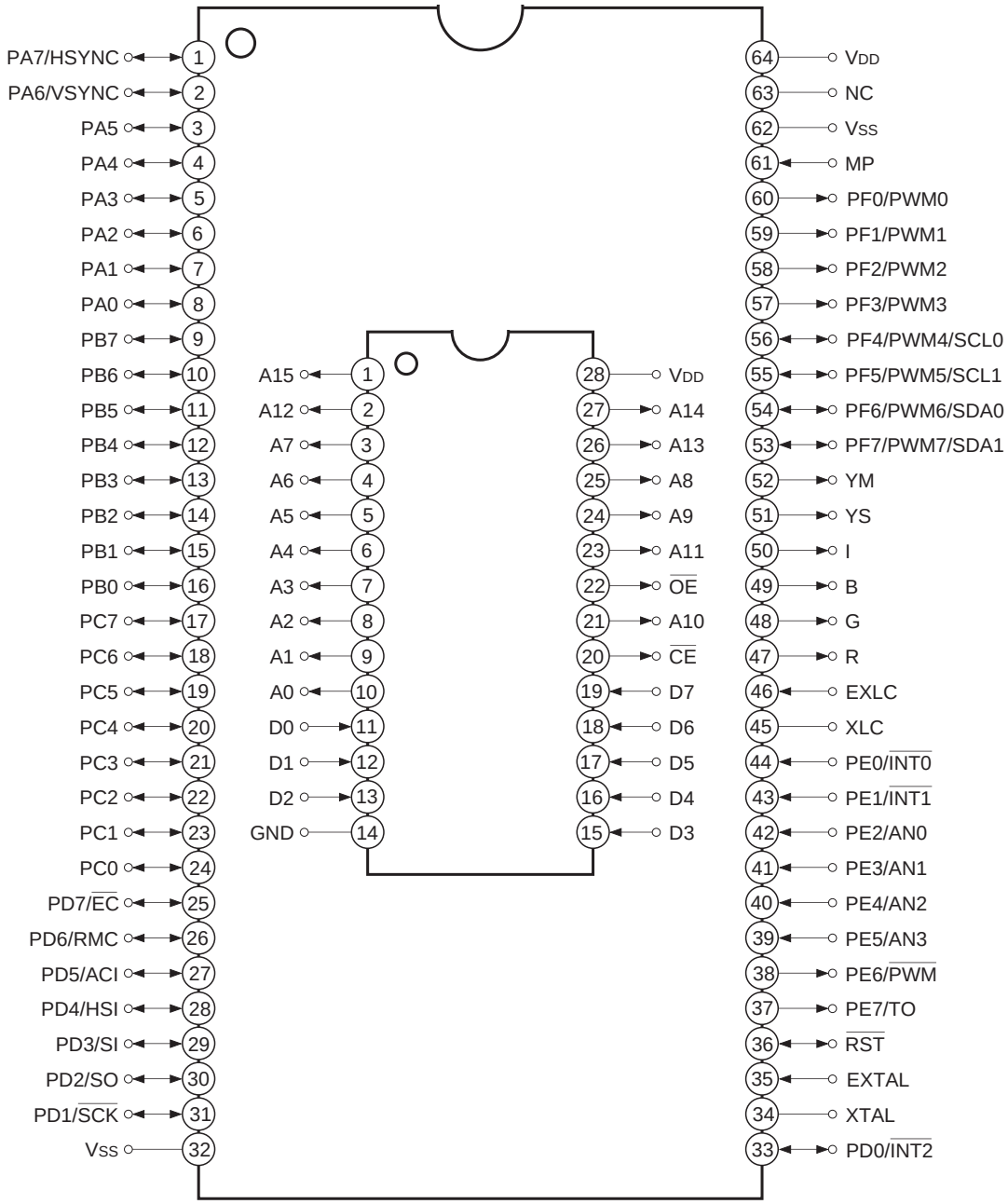
Note) Optional mask depends on the type of the CXP85300A/85390A. Refer to the product list for details.

E94334A7Z-PS

CXP85300A

Pin Assignment: Piggyback mode 1

(Top View) 64 pin PSDIP Package

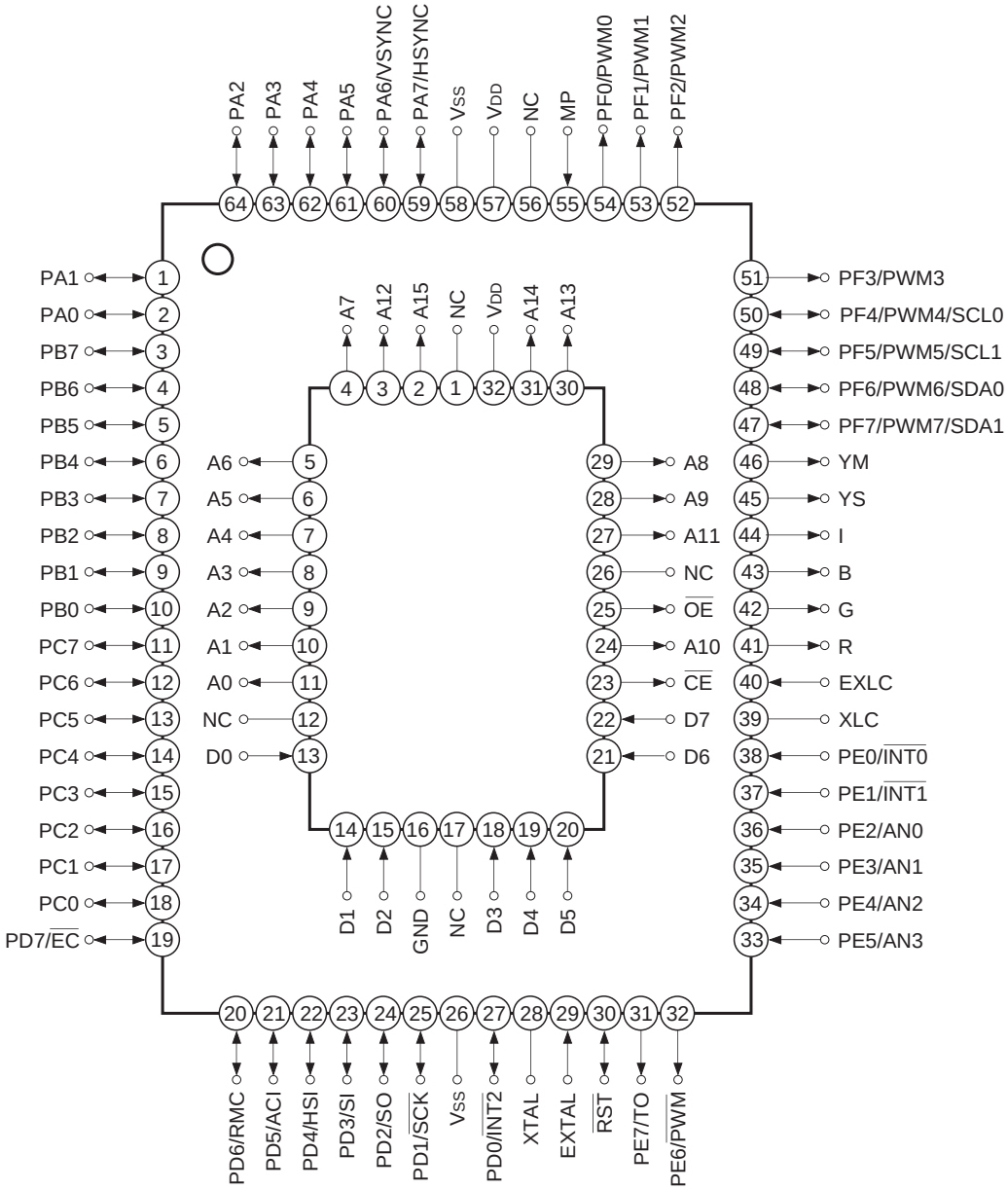


Note) 1. NC (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are always connected to GND.
3. MP (Pin 61) is always connected to GND.

CXP85300A

Pin Assignment: Piggyback mode 2

(Top View) 64 pin PQFP Package

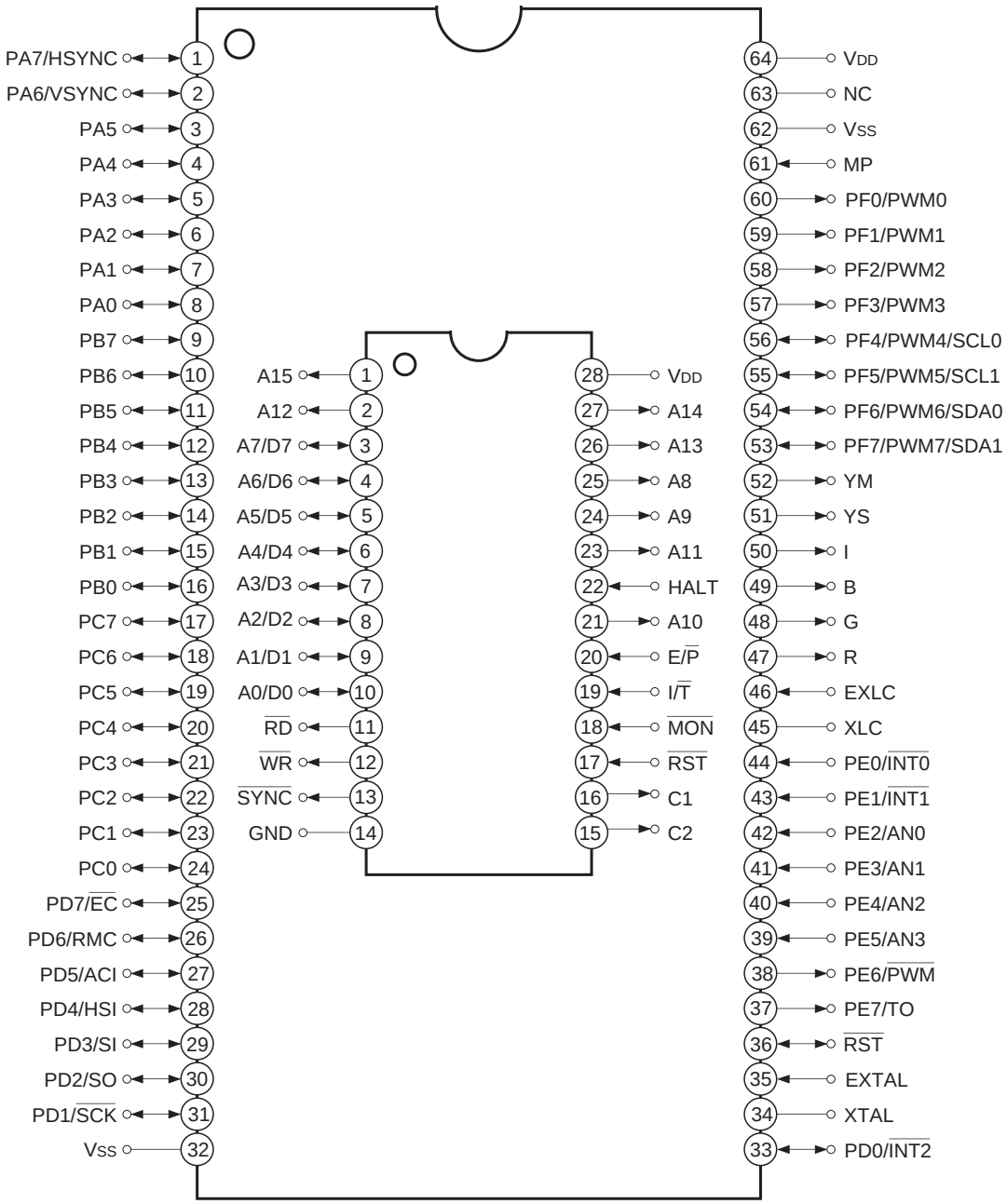


Note) 1. NC (Pin 56) is always connected to V_{DD}.
2. Vss (Pins 26 and 58) are always connected to GND.
3. MP (Pin 55) is always connected to GND.

CXP85300A

Pin Assignment: Evaluator Mode 1

(Top View) 64 pin PSDIP Package

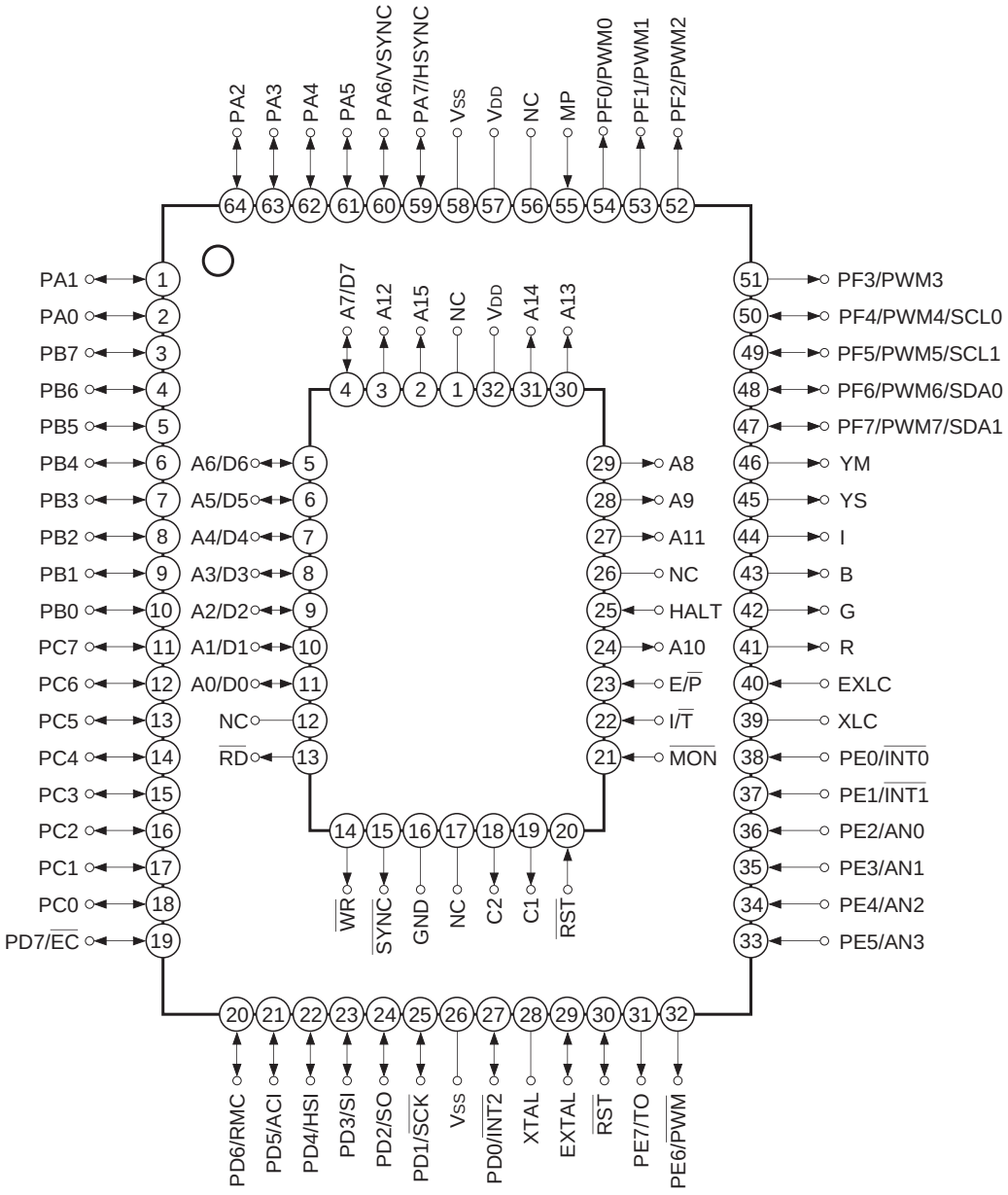


Note) 1. NC (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are always connected to GND.
3. MP (Pin 61) is always connected to GND.

CXP85300A

Pin Assignment: Evaluator Mode 2

(Top View) 64 pin PQFP Package



Note) 1. NC (Pin 56) is always connected to V_{DD}.
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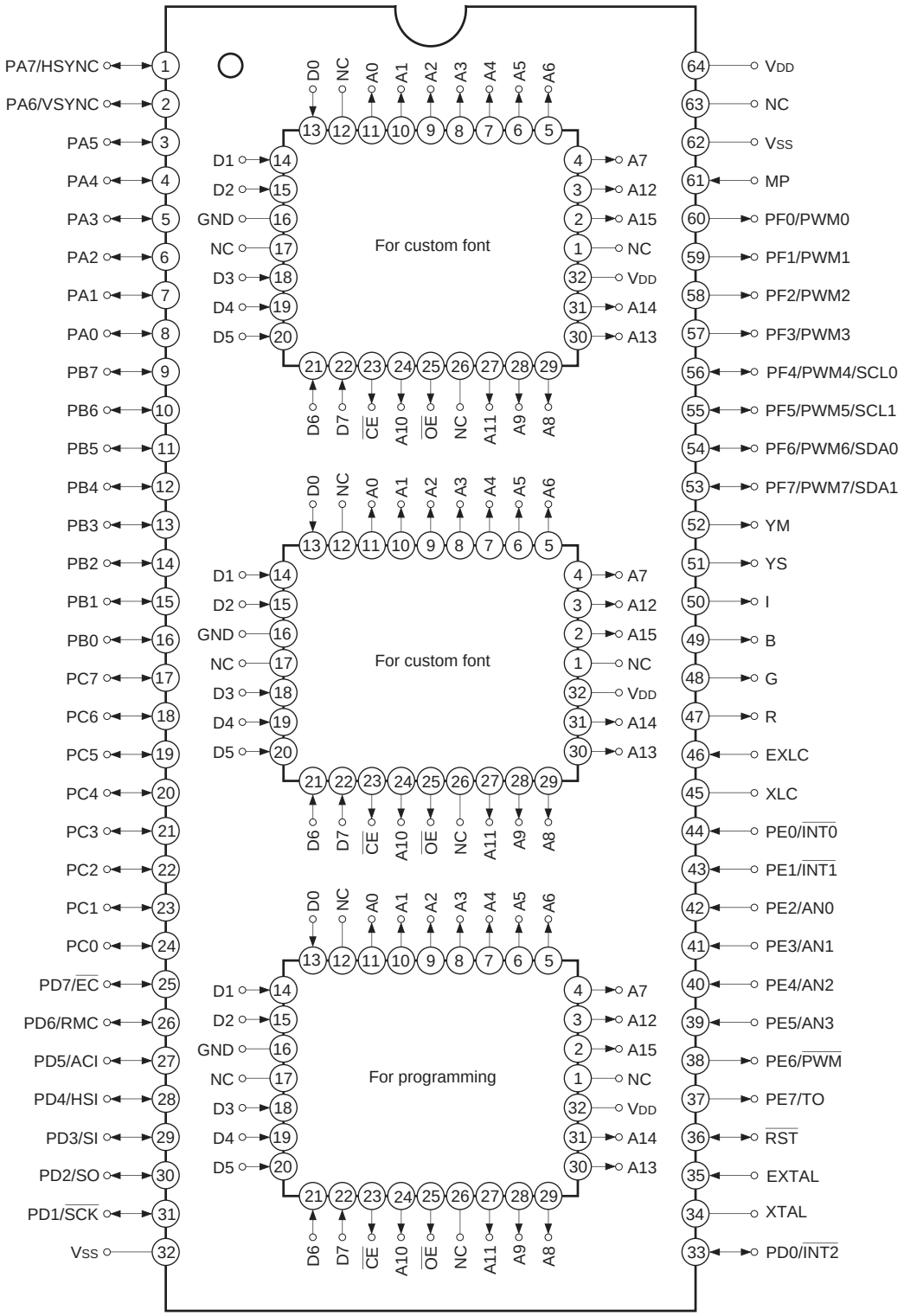
CXP85390A

Pin Assignment: Piggyback Mode

(Top View) 64 pin PSDIP Package



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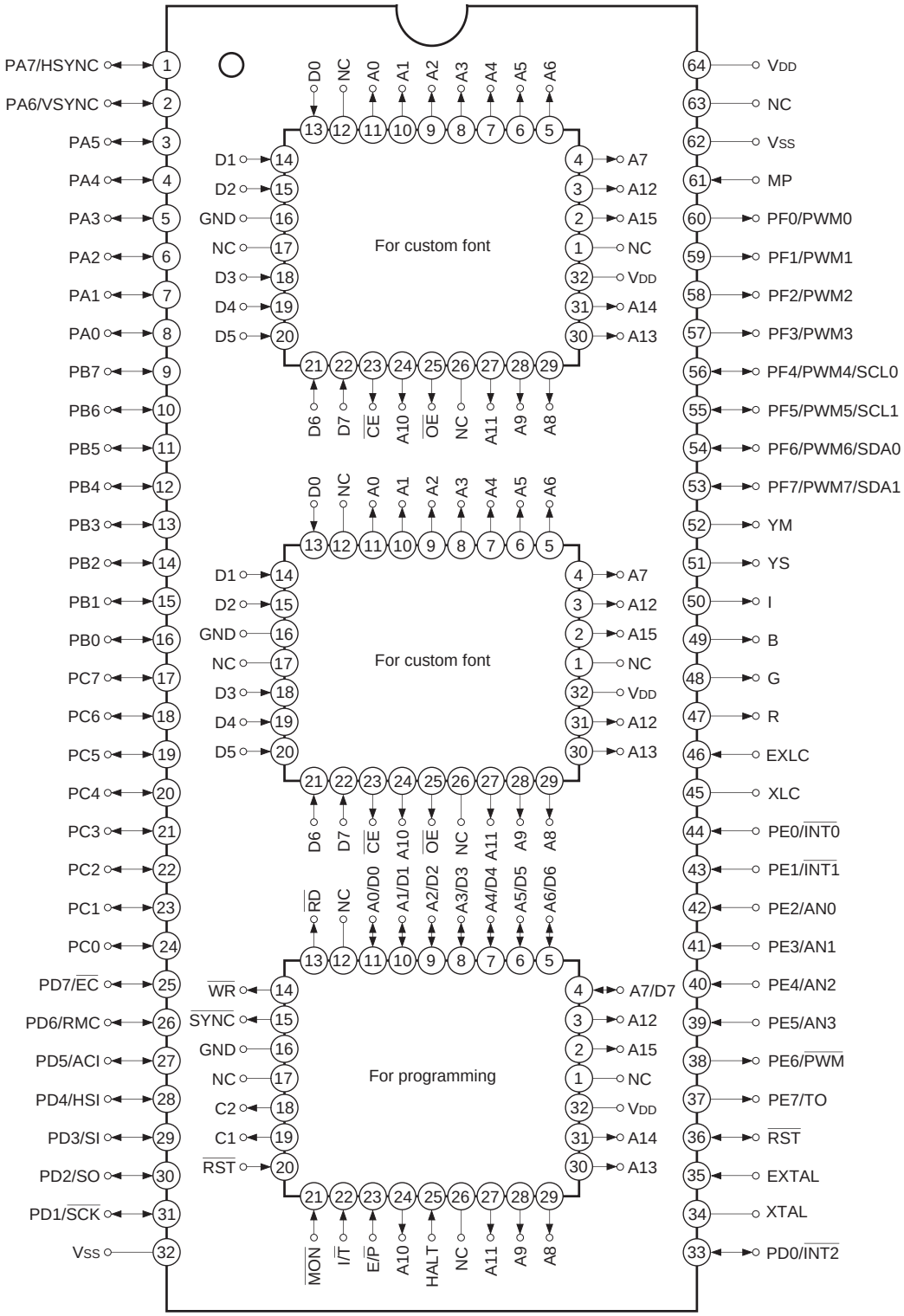
CXP85390A

Pin Assignment: Evaluator Mode

(Top View) 64 pin PSDIP Package



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3. MP (Pin 61) is always connected to GND.

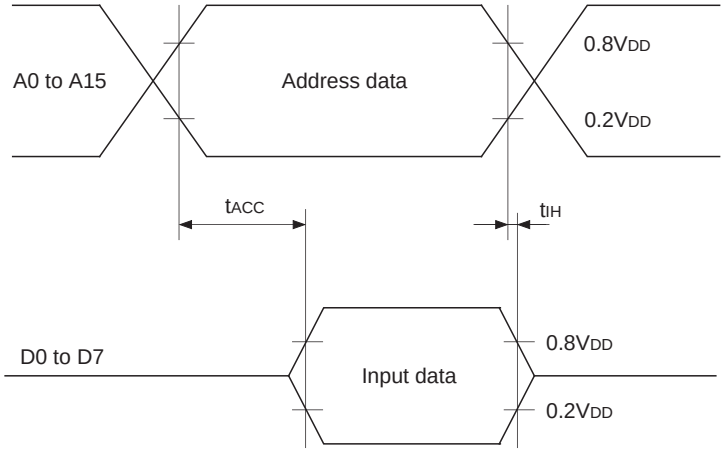
EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		150*1	ns
				250*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 Oscillator clock 8MHz version

*2 Oscillator clock 4MHz version

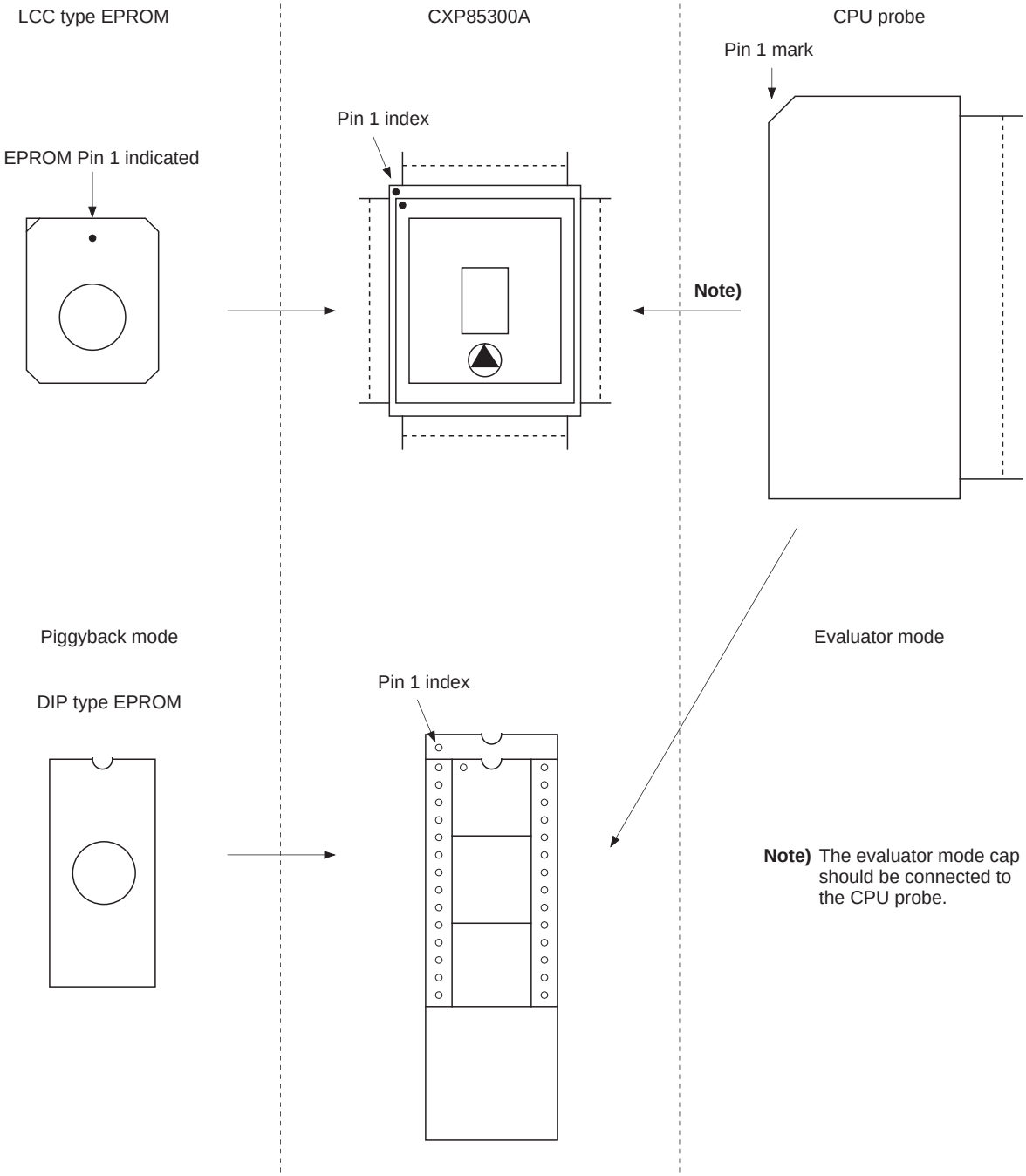


Product List

Optional item	Product						
	Mask			Piggyback/evaluator			
	CXP85324A	CXP85332A	CXP85340A	CXP85300A-U02S CXP85300A-U02Q	CXP85300A-U03S CXP85300A-U03Q	CXP85390A-U02S	CXP85390A-U03S
Package	64 pin plastic SDIP/QFP			64 pin ceramic PSDIP/PQFP		64 pin ceramic PSDIP	
Oscillator clock	4MHz/8MHz			4MHz	8MHz	4MHz	8MHz
ROM capacity	24K bytes	32K bytes	40K bytes	EPROM 40K bytes			
Reset pin pull-up resister	Existent/Non existent			Existent			
Power-on reset circuit	Existent/Non existent			Existent			
Font data	User data			Fixed		EPROM 16K bytes	

CXP85300A

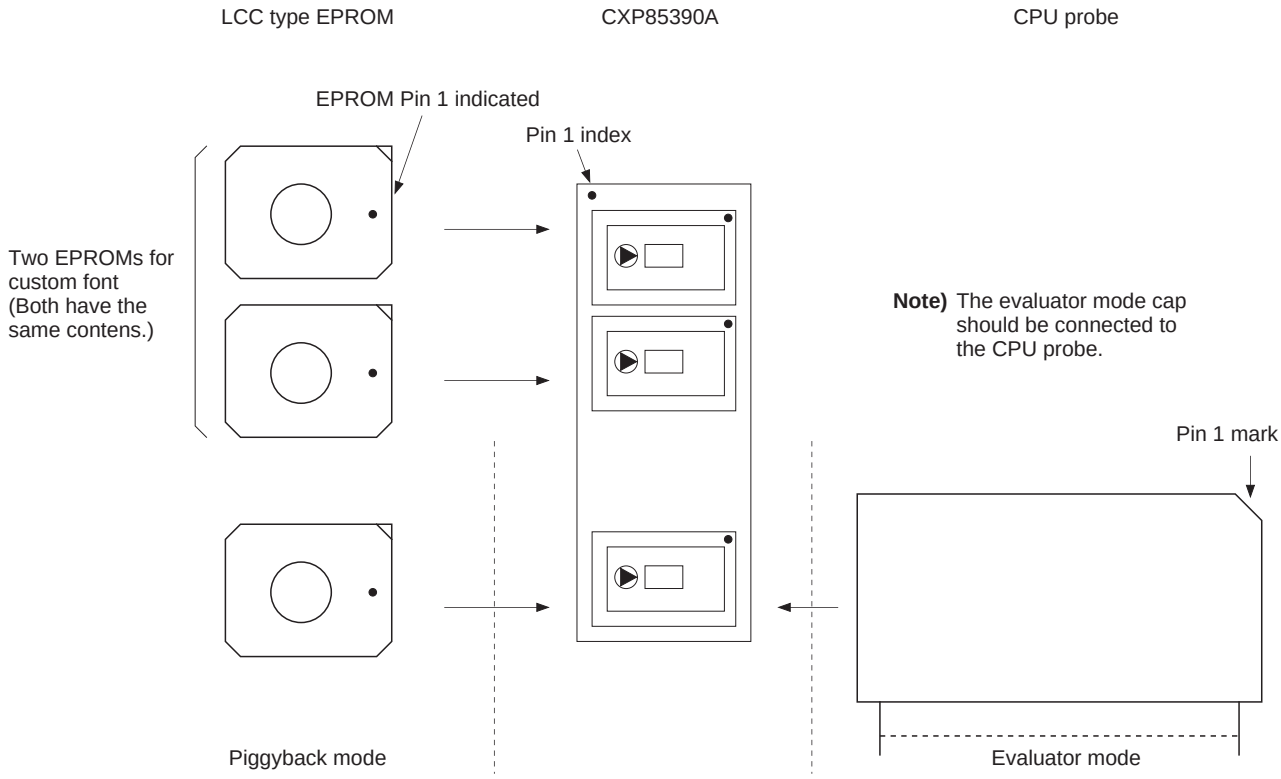
Piggyback mode/evaluator mode switching process is as follows.



Note) The evaluator mode cap should be connected to the CPU probe.

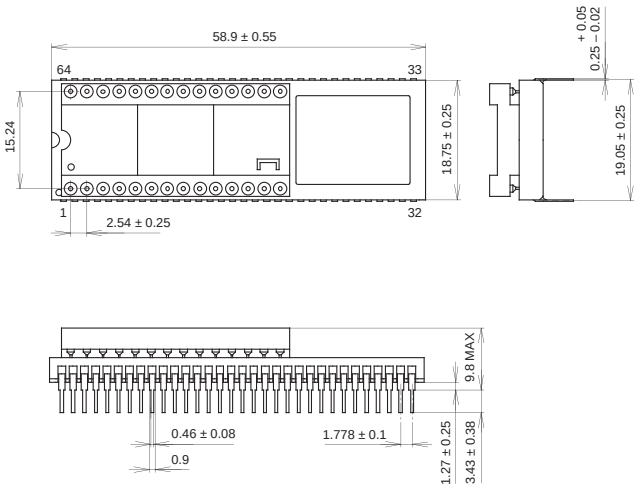
CXP85390A

Piggyback mode/evaluator mode switching process is as follows.



Package Outline Unit: mm

64PIN PSDIP (CERAMIC) 750mil

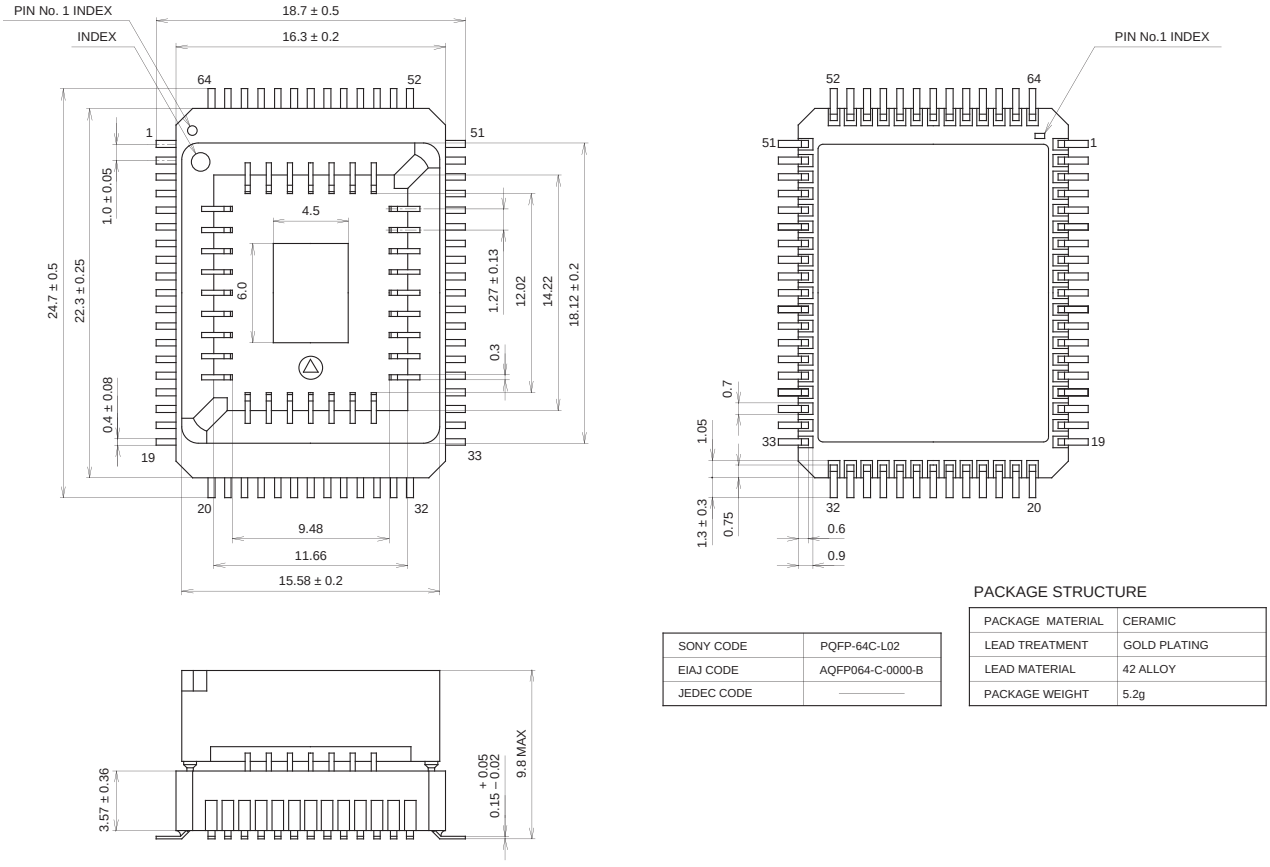


PACKAGE STRUCTURE

SONY CODE	PSDIP-64C-01
EIAJ CODE	ADIP064-C-0750-A
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	16.0g

64PIN PQFP (CERAMIC)

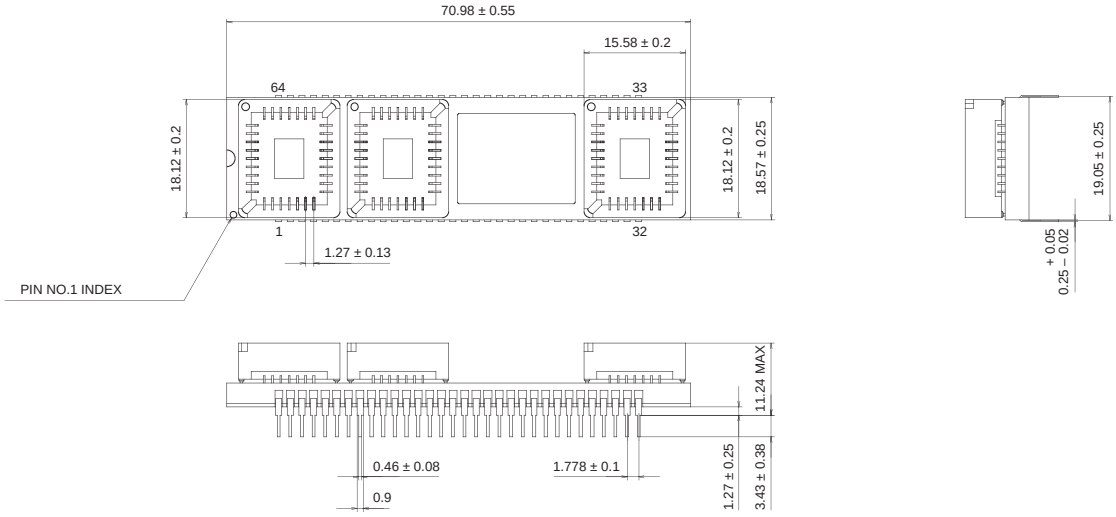


PACKAGE STRUCTURE

SONY CODE	PQFP-64C-L02
EIAJ CODE	AQFP064-C-0000-B
JEDEC CODE	————

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g

64PIN PSDIP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PSDIP-64C-02
EIAJ CODE	ADIP064-C-0750-B
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	22.8g